Obtaining the High-resolution Epoch with the FPGA Technology

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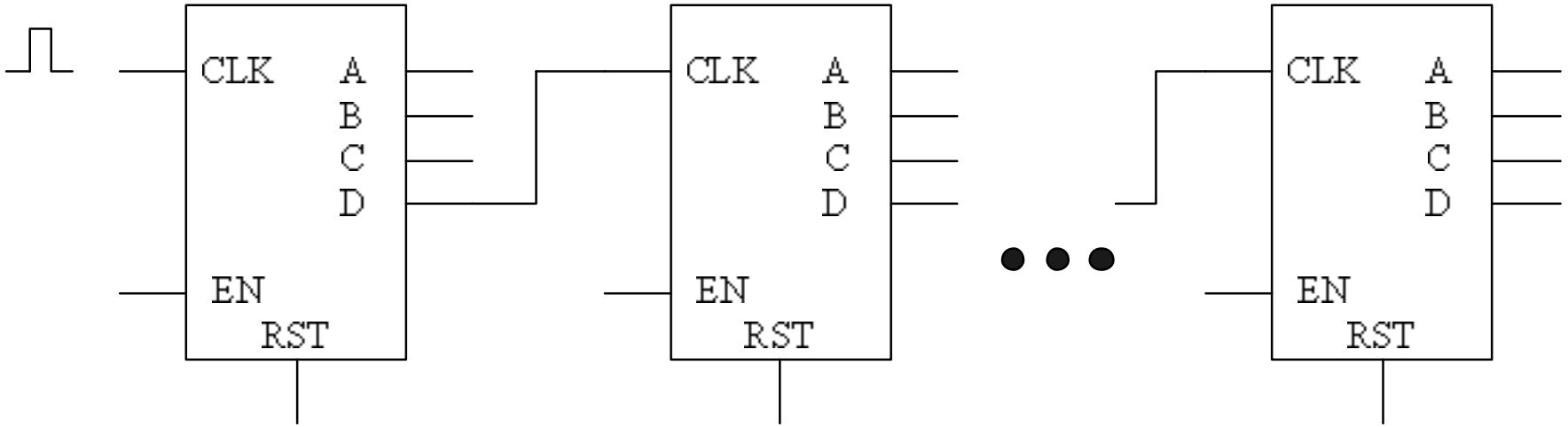
Goals

- Record the transmission epoch of a laser pulse
- Achieve the resolution to 100ns or higher

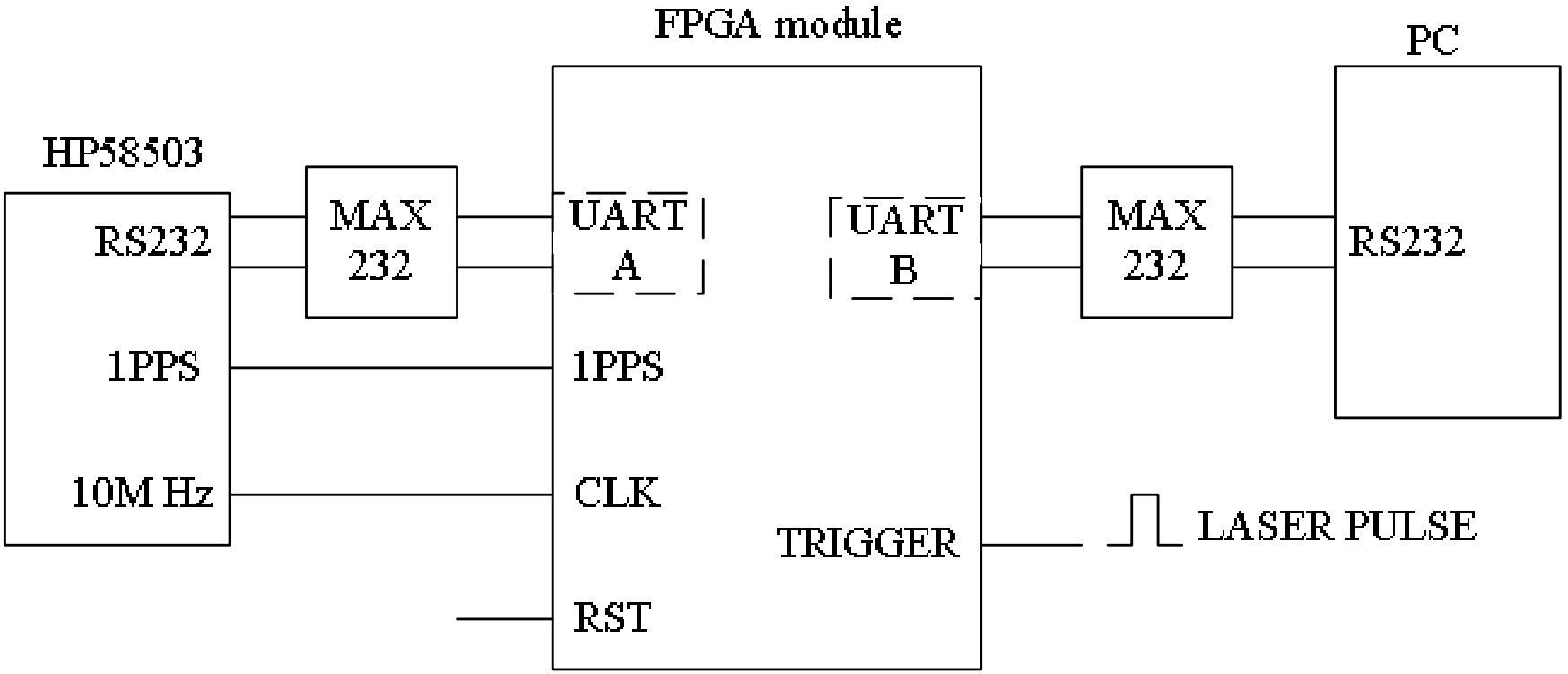
The module running

- Cascade connection of counters



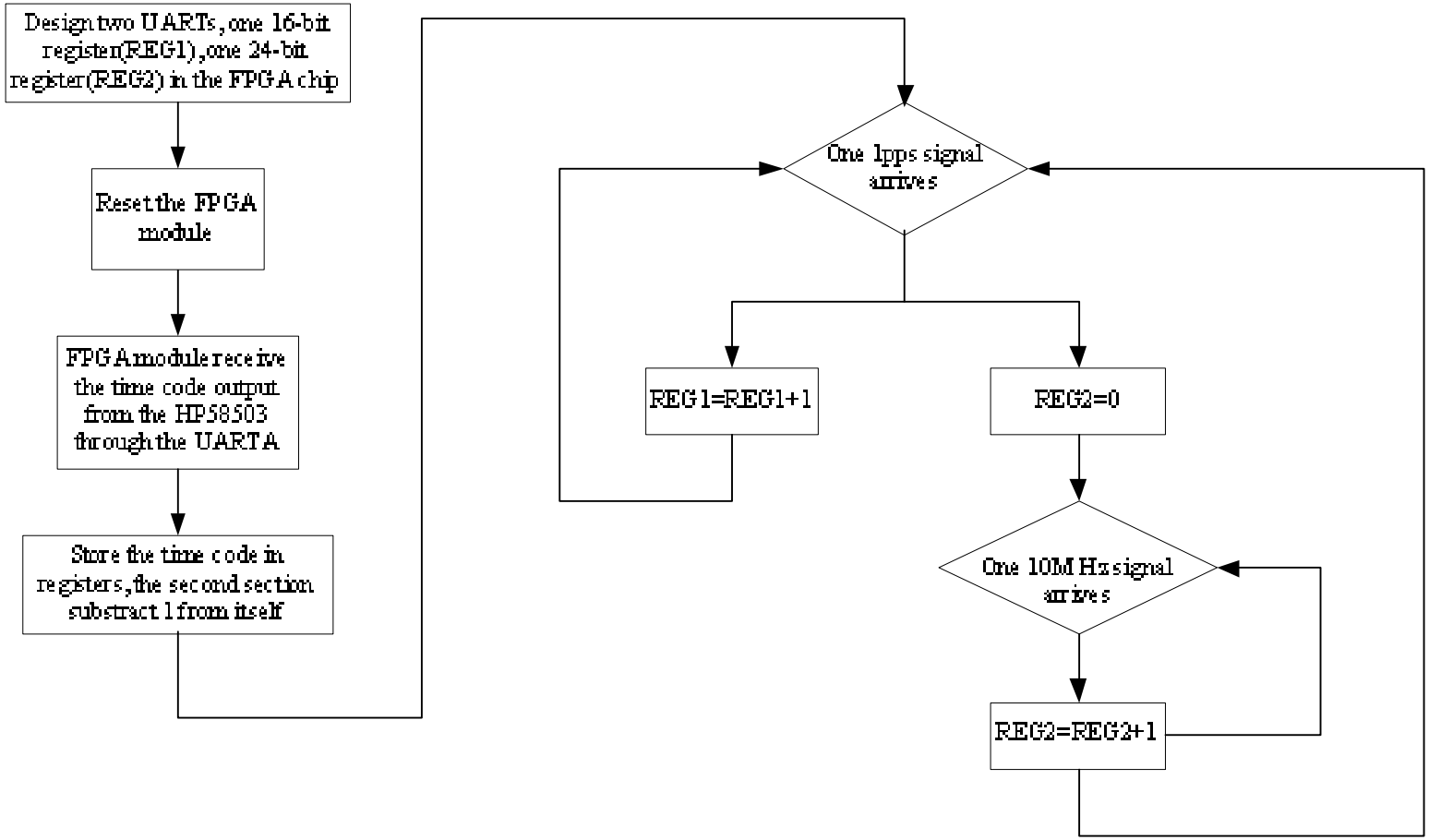
The module with FPGA-1/3

- System composition



The module with FPGA-2/3

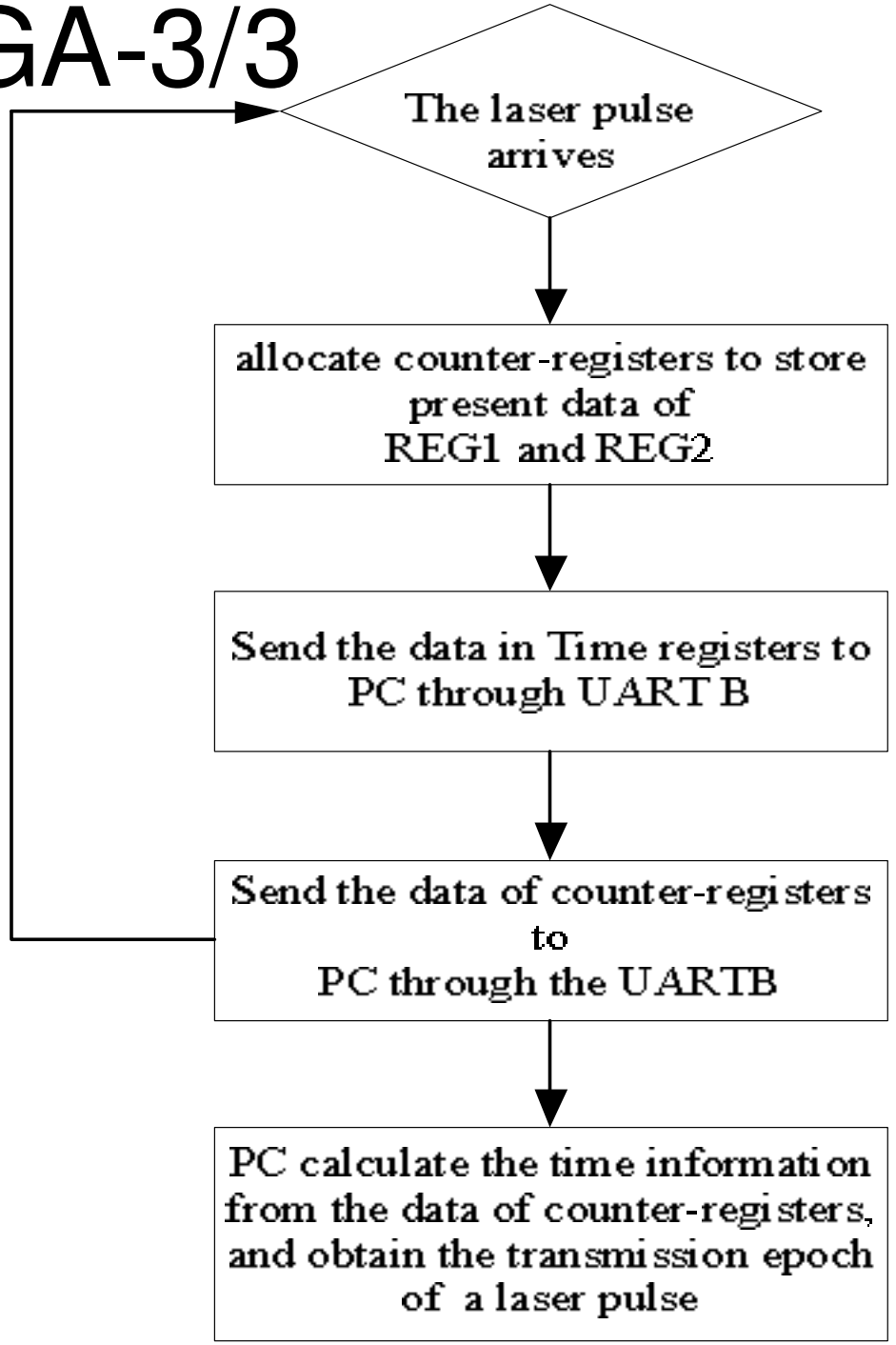
- **The realization of timing**



  - **REG1 store the section whose unit is second**
  - **REG2 stroe the section in 1 second, and must have 24 bits at least**

The module with FPGA-3/3

- Record the transmission epoch of a laser pulse
  - –With this flow, the frequency of laser pulse can't be very high, otherwise a EEPROM chip is needed to restore the data.



Development flat

- Hardware:
  - Xilinx's Spartan III FPGA
- Software:
  - Xilinx ISE 7.1
  - VC6.0 ++
- Top-level Module type
  - HDL(Verilog HDL)
- Simulator
  - ISE Simulator
- Synthesis
  - XST(VHDL/verilog)

Conclusion

- Using the 10M Hz output (sine wave) of HP58503 as the clock input of the FPGA module is feasible
- The module can obtain the epoch with resolution to 100 ns, and higher resolution can be also achieved with a frequency multiplication module added to the FPGA

Next to do

- Reform the control module with FPGA to achieve higher resolution, precision, stability, flexibility, expansibility and integrated level.
- Considering the respective advantages and disadvantages of MCU and FPGA, the structure “MCU+FPGA” may help us to reduce the development time. So it’s valuable to try.

THANK YOU